TITLE	DOC No. RFD-20261111100-001	
400G QSFP-DD 400G SR8 Transceiver	REVISION：01	AUTHORIZED BY：Henry Chen
	DATE：2026.11.11	CLASSIFICATION：Optical Transceiver

1. Features and Benefits

- Eight-channel full-duplex transceiver
- 8x53.125Gb/s electrical interface
- Maximum link length of 70m on OM3 (MMF), 100m on OM4 (MMF)
- Power dissipation < 8W
- Built-in digital diagnostic functions
- 850nm VCSEL transmitter
- Good EMI performance
- Single 3.3V power supply
- RoHS compliant
- built-in DSP
- Operating case temperature: 0 ~ +70°C

2. Product Description

The QSFP-DD 4*100Gbps transceiver module is an assembly of eight full-duplex lanes, where each lane is capable of transmitting data at rates up to 26.5625GBd each lane. It is compliant to QSFP-DD MSA Rev5.0, and Common Management Interface Specification Rev4.0.

2.1 Product Name

QSFP-DD 400G SR8 100m transceivers

JPC P/N	Data Rate	Wavelength (nm)	Distance	Power(dBm)	Sen.(dBm)	Connector	Temp.
P68**8GRCAM1-1	4x100G	850	70m (OM3) 100m (OM4)	-8.4 ~ 2.4	-8.4	MPO-16	C

Note-1：** Indicates the customer code.

JPC connectivity

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2.2 Mechanical Specifications

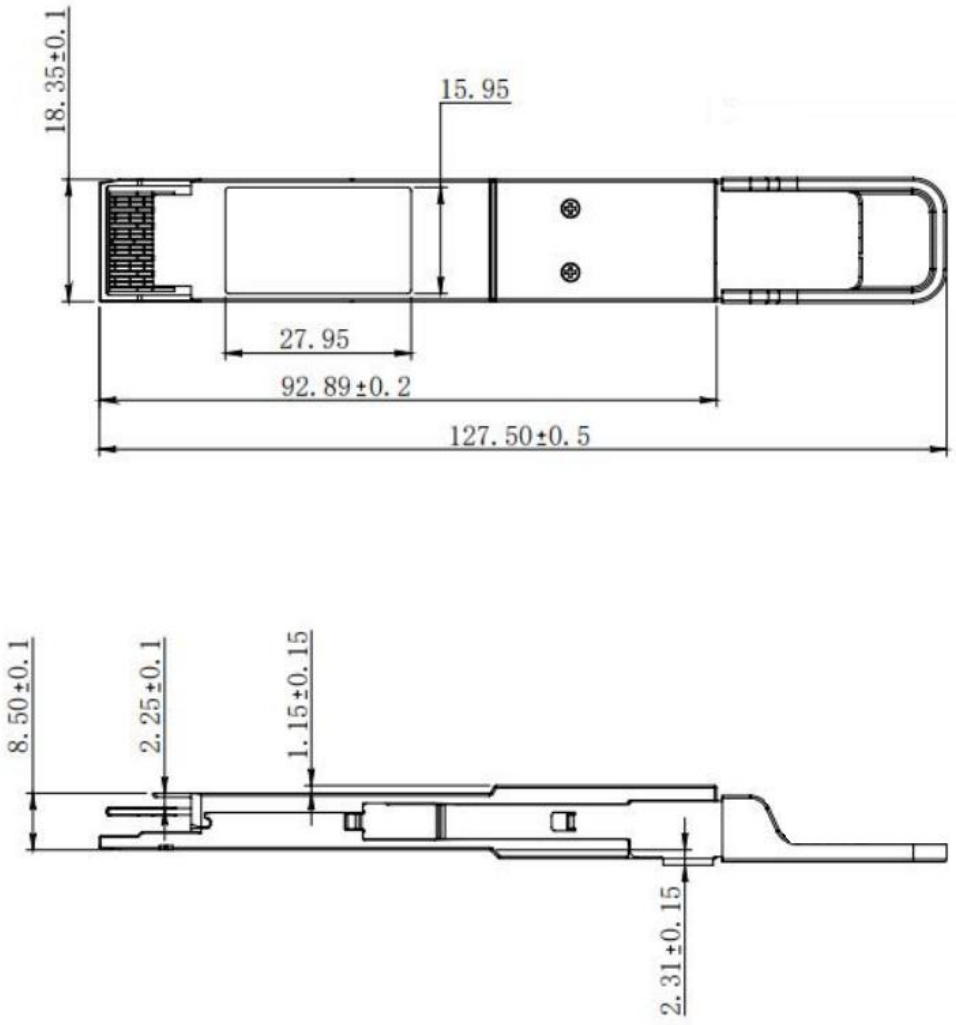


Figure 1 – QSFP-DD Mechanical Specifications (unit: mm)

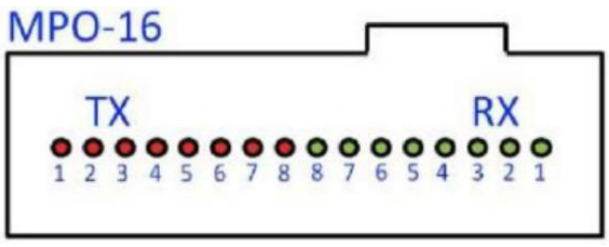


Figure 2 – QSFP-DD Optical lanes Assignment

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3. ABSOLUTE MAXIMUM RATINGS (TC=25°C, UNLESS OTHERWISE NOTED)

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings will cause permanent damage and/or adversely affect device reliability.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Storage Temperature	TS	-40	-	+85	ºC	
Maximum Supply Voltage	Vcc	-0.3	-	3.6	V	
Operating Relative Humidity	RH	10	-	+85	%	

4. RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Data Rate（each lan）	DR		26.5625		GBd	
Bit Error Rate	BER			2.4E-4		
Operating Case Temperature	Tcase	0		70	ºC	
Fiber Length on MMF(OM4)	L			100	m	OM4

5. PIN DESCRIPTIONS

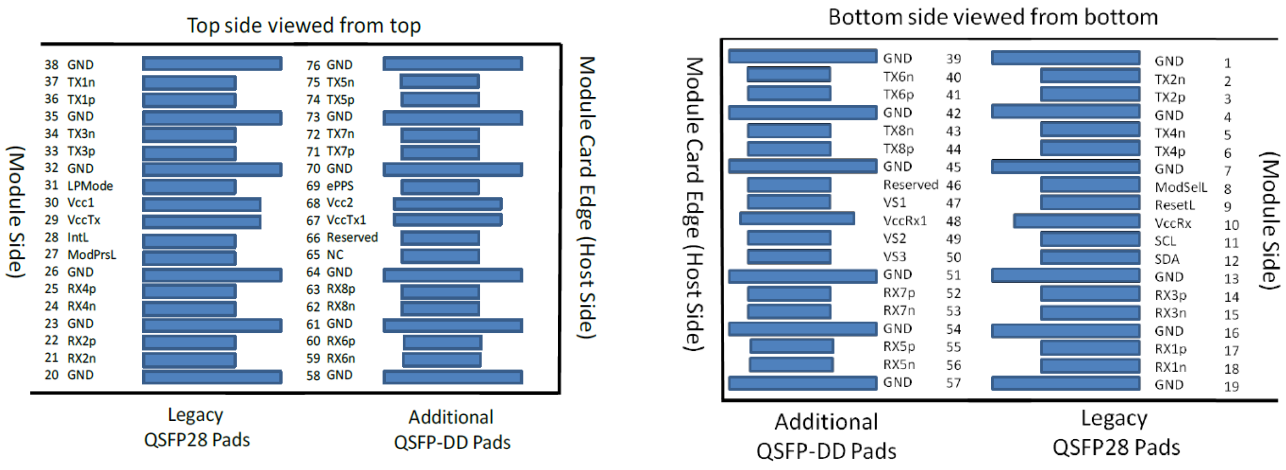


Figure 3 – Pin Definitions

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select.	3B	
9	LVTTL-I	ResetL	Module Reset.	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present.	3B	
28	LVTTL-O	IntL	Interrupt.	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power Mode	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference	3A	3

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Pad	Logic	Symbol	Description	Plug Seq[4]	Notes
			clock input		
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

[1] QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

[2] VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

[3] All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

[4] Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

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6. LOW SPEED CONTROL AND SENSE SIGNALS

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc*0.3	V	
	VIH	VCC*0.7	Vcc+0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0 k Ohms Pullup resistor, max. For 1000kHz clock rate refer to Figure 45
			200	pF	For 400kHz clock rate use 1.6 k Ohms pullup resistor, max. For 1000kHz clock rate refer to Figure 45.
LPMode, ResetL, ModSelL and ePPS	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
LPMode, ResetL and ModSelL	|Iin|		360	uA	0V<Vin<Vcc
ePPS	|Iin|		TBD	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
	VOH	VCC-0.5	VCC+0.3	V	10k Ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0 mA
	VOH				ModPrsL can be implemented as a short-circuit to GND on the module

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7. ELECTRICAL SPECIFICATION

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Tx Data Differential Input Voltage	Vin	-	-	900	mV	
Tx Data Differential Input Impedance	Zin	-	100	-	Ohm	
Receiver						
Rx Data Differential Output Voltage	Vout	-	-	900	mV	
Rx Data Differential OutputImpedance	Zout	-	100	-	Ohm	

8. OPTICAL SPECIFICATION

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter						
Signaling rate per lane		26.5625±100ppm			GBd	1
Center wavelength	λ	840	850	860		
RMS Spectral Width	SW			0.6	nm	
Transmit OMA per Lane	TXP	-6.4		3	dBm	
Transmit Average Power per Lane	Pout	-8.4		2.4	dBm	
Transmitter and dispersion eye closure for PAM4 (TDECQ), each lane	TDECQ			4.5	dB	
Optical Extinction Ratio	ER	3			dB	
Average launch power of OFF transmitter, per lane				-30	dBm	
Optical return loss tolerance	RL			12	dB	
Receiver						
Signaling rate per lane		26.5625±100ppm			GBd	1
Damage Threshold	DT	3.4			dBm	
Average Receive Power per Lane	RXP	-8.4		4	dBm	
Average Receive sens per Lane	RXPsens			-8.4	dBm	2.4E-4
Receive Power (OMA) per Lane	RxOMA			3	dBm	
Receiver Reflectance	Rfl			-12	dB	

Notes:

[1] Transmitter and Receiver consists of 8 lasers and photodiode operating at 26.5625GBd each.

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9. Module Memory Map

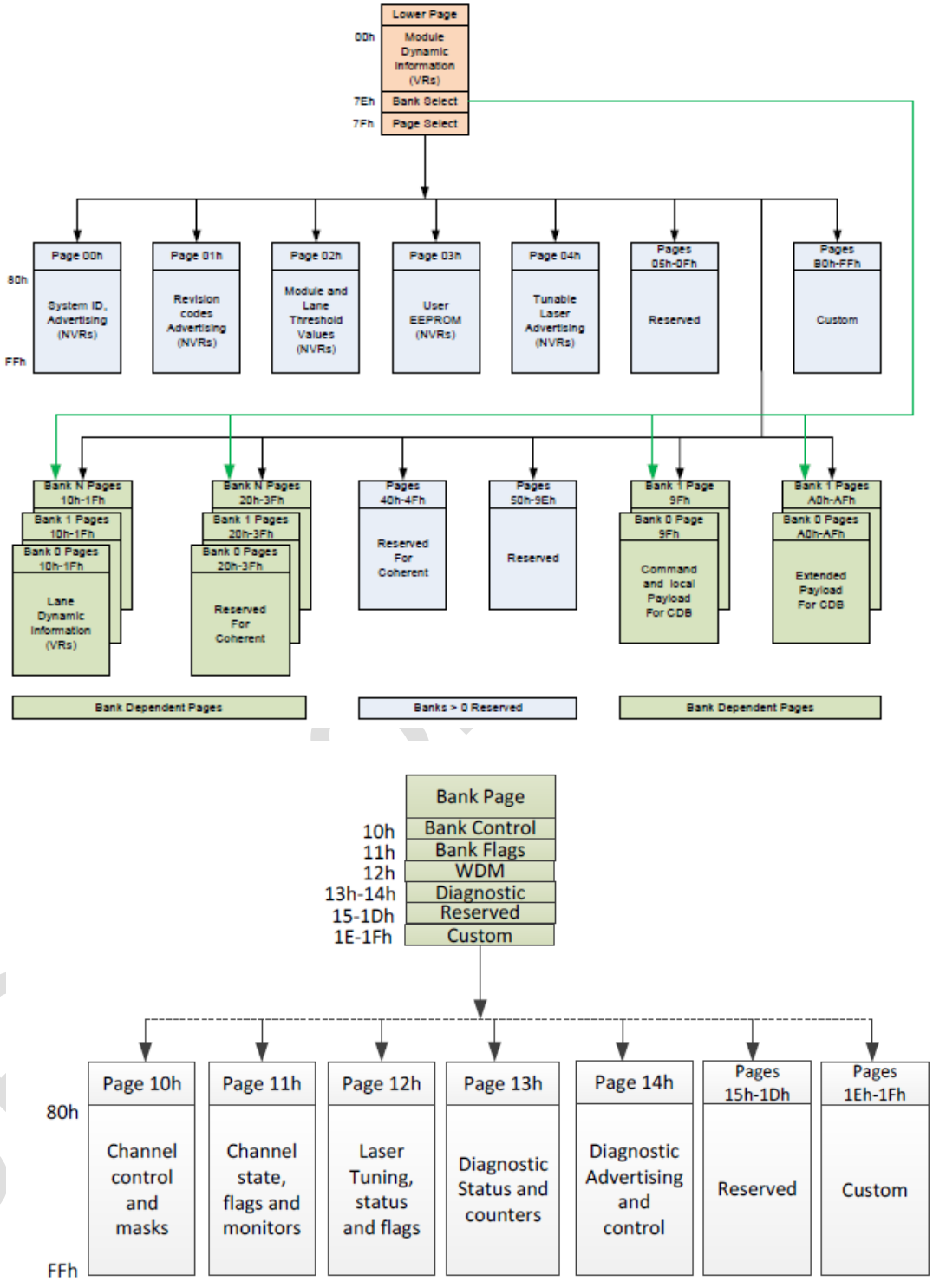


Figure 4 – QSFP-DD Memory Map

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10. DIGITAL DIAGNOSTIC SPECIFICATION

Parameter	Symbol	Accuracy	Units	Notes
Transceiver Case Temperature	DMI_TEMP	±3	℃	Over operating temp
Supply voltage monitor absolute error	DMI _VCC	±3%	V	Full operating range
Channel Bias current monitor	DMI_IBIAS	±3%	mA	Per channel
Channel RX power monitor absolute error	DMI_RX	±3	dB	Per channel
Channel TX power monitor absolute error	DMI_TX	±3	dB	Per channel

11. Modification History

Rev.	Comments	Date	Originator	Approval
01	Preliminary draft	2026.11.11	Henry Chen	Mike Sun

JPC connectivity